Powering Celeron-type microprocessors using TI's TPS5210 and TPS5211 controllers

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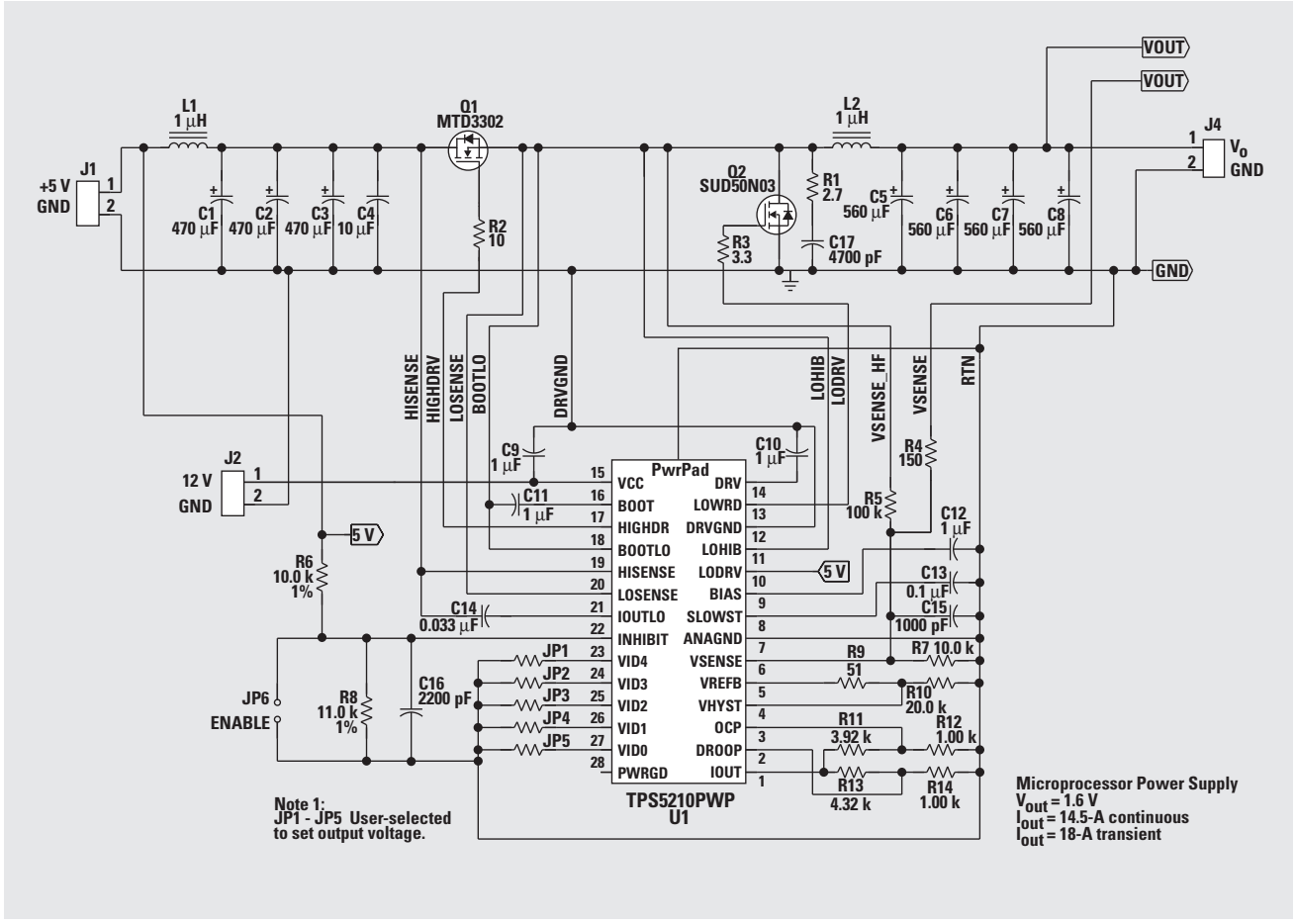
Introduction

Performance of desktop application microprocessors is improving rapidly, approaching the requirements that were typical for servers and workstations just a few years ago. In this high-performance PC, the voltage regulator has to supply the high current consumed by the microprocessor core to keep the core voltage within tight static and dynamic tolerances for minimum cost. The TPS5210EVM-147 (SLVP147) evaluation module has been designed and tested to confirm TI's TPS5210 and TPS5211 hysteretic controller performance to supply future Celeron™ microprocessors. The SLVP147 includes a synchronous DC-DC buck converter, high-frequency decoupling capacitors for PGA-370 microprocessor packages, and a load-current transient tester. The DC-DC converter has 5-V input and 1.6-V output voltage and requires 12 V, 30 mA for the controller itself. It was designed as a low-cost solution in motherboard applications where small size is very important. The temperature of the components does not exceed 72°C at room ambient temperature with a load current of 14.5 A. The module has excellent transient characteristics at a peak load current of up to 18.4 A. A four-layer PCB had been used in the module to get electrical and temperature conditions close to actual conditions. The module meets electrical specifications of the Intel document "VRM 8.4 DC-DC Converter Design Guidelines" for >733-MHz clock and 133-MHz bus-frequency Celeron processors.

Figure 1. DC-DC synchronous buck converter schematic



For this application R5 is open.

Brief description of the SLVP147 evaluation module

Several evaluation modules for different desktop motherboard applications have been designed. The description and characteristics of one of them is presented in this report.

The SLVP147 evaluation module (4" x 3.25" x 0.8") includes three main parts:

- 1.6-V power supply (2" x 1.5" x 0.8"),
- Processor bypass capacitors, and
- Transient load.

The four-layer, 1-oz. FR-4 PCB board, which is typical for motherboards, had been used in the module to simulate actual application conditions for an embedded point-of-load power supply.

1.6-V power supply

The 1.6-V power supply is a DC-DC synchronous buck converter (see the schematic in Figure 1 and lower right corner of the evaluation module in Figure 2) that includes input and output filters, power stage, and control section.

The input voltage for the power section is 5 V ± 0.5 V, and the control section requires 12 V ± 0.6 V. All power-supply components are placed in the corner of the board to model the worst-case cooling conditions. Because of

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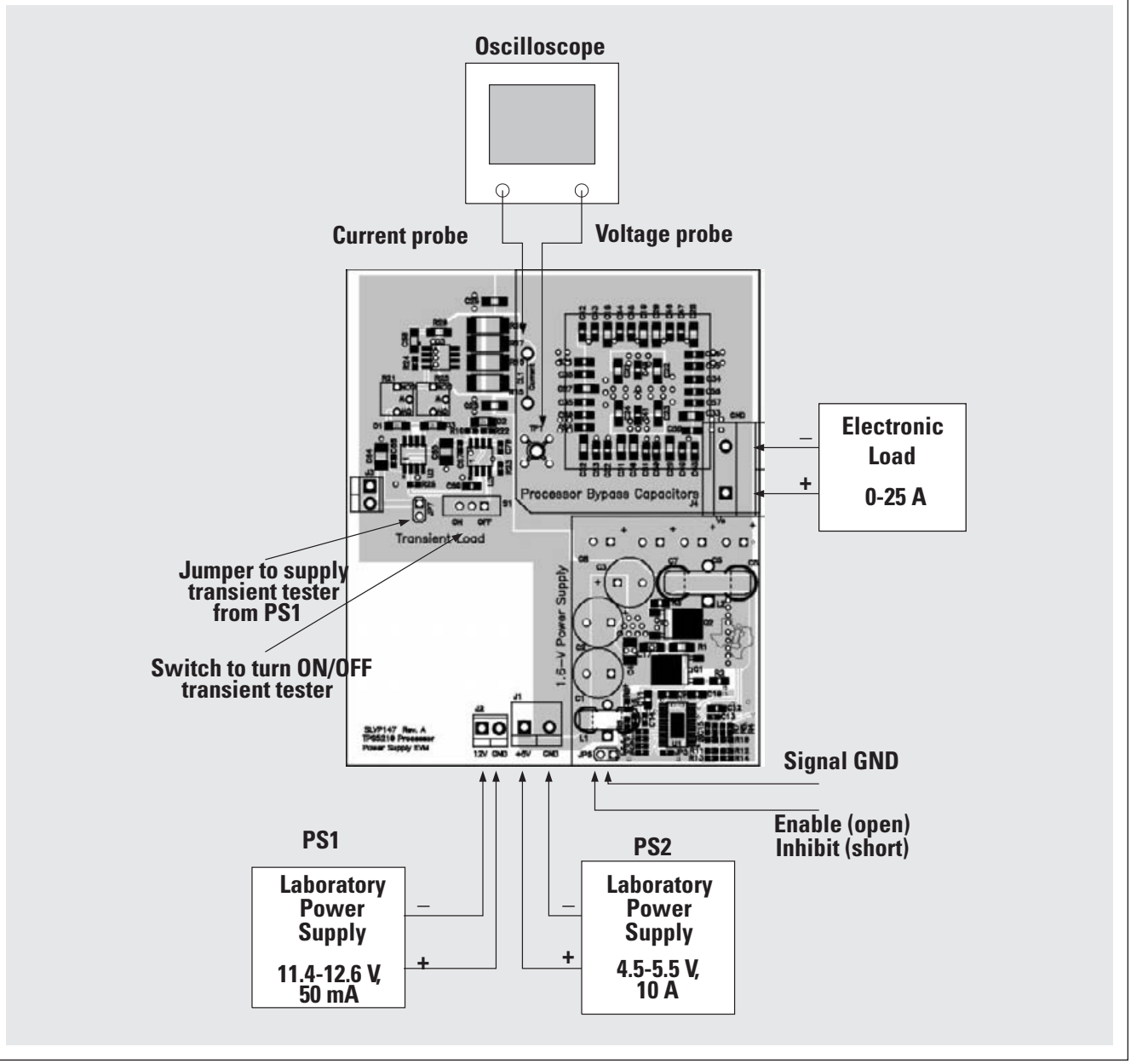
Figure 2. Test setup for SLVP147 EVM



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minimum size requirements, high-performance OS-CON-type capacitors have been selected for the input and output filters. The input filter includes three 10SP470M capacitors C1–C3, 10-µF ceramic capacitor C4, and 1-µH inductor L1. The input capacitors can handle a total maximum RMS current as high as 13.5 A. The output filter has four OS-CON-type capacitors (4SP560M) and a 1-µH inductor, L2. The fast hysteretic controller and active droop reduce the number of capacitors while having a reliable margin for dynamic tolerance. The power stage includes power FETs in DPAK packages Q1, Q2, gate resistors R2 and R3, and snubber circuitry including resistor R1 and capacitor C17. The selection of a 10-MΩ MTD3302 high-side FET and a 7-MΩ SUD50N03-07 low-side FET is a compromise between cost and efficiency.

The controller section is based on the high-performance TPS5210 hysteretic controller and provides the following main functions:

- Adaptive dead-time-control high- and low-side drivers with an 8-V drive regulator and internal bootstrap diode to switch power FETs with minimum control and switching losses
- A sample-hold circuit to sense the V_{ds} of the high-side FET for shutdown overcurrent protection and active droop compensation without expensive external current sensors
- A fast hysteresis comparator, which does not need feedback loop compensation circuitry that reacts to transients in 400–500 ns without restrictions on duty cycle (the hysteresis window is set by an external resistor as a percentage of the reference voltage)
- A 5-bit VID code, enable/inhibit signal input, power good signal, undervoltage lockout for both 12-V and 5-V inputs, and overvoltage shutdown

Processor bypass capacitors

The high-frequency decoupling capacitors (see the upper right corner of the evaluation module in Figure 2) occupy the same area as the cavity of the PG-370 package to model real-load current transient conditions. The decoupling circuitry includes 27 ceramic 0805 1-µF capacitors and 16 ceramic 4.7-µF capacitors in 1206 packages. Test point

Table 1. VRM 8.4 requirements and test data

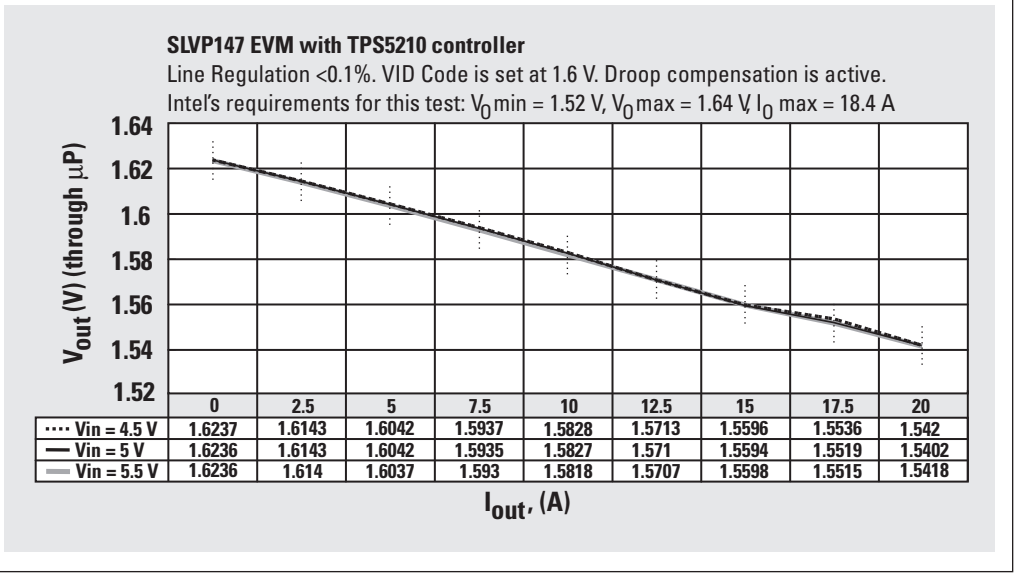
TEST	DESCRIPTION	SPECIFICATION	DATA
1	Operating voltage and load current (VRM 8.4. sections 1.1 and 1.2)	Input voltages 4.75 to 5.25 VDC and 11.40 to 12.6 VDC. Load current 0 to 18.4 A	Unit operates over the full input-voltage and load-current range at switching frequency 135 to 175 kHz (Figure 7)
2	Steady-state output voltage (VRM 8.4. section 1.1)	Output voltage within 1.52 to 1.64 VDC	Output voltage over the full input-voltage and load-current range within 1.551 to 1.624 V including droop compensation. Temperature regulation and set point < 1% (Figure 3).
3	Transient output voltage (VRM 8.4. section 1.1)	Output voltage within 1.52 to 1.65 VDC at load-current steps in 0.8- to 18.4-A range with 20-A/µs slew rate	Output voltage within 1.552 to 1.644 V, response time < 500 ns, recovery time < 7 µs for step-up and < 34 µs for step-down (Figures 4 and 5)
4	Output ripple and noise (VRM 8.4. section 1.1)	Included in steady-state output-voltage requirements. Measured with 20-MHz frequency band.	20-mV peak-to-peak maximum (Figure 6)
5	Turn on overshoot (VRM 8.4. section 1.1)	< 10%, no load and full load	< 1.3% at all load conditions (Figure 11)
6	Turn on response time (VRM 8.4. section 1.1)	< 10 ms	< 9 ms (Figure 11)
7	Power good signal (VRM 8.4. section 1.1)	High if the output voltage exceeds ±12% from nominal; otherwise low, transition to high within 20 ms	±12% from nominal, guaranteed by controller design
8	Output enable (VRM 8.4. section 1.3)	Open-collector input signal	Guaranteed by controller design (Figure 11)
9	5-bit VID (VRM 8.4. section 1.3)	Input open-collector TTL signals	Guaranteed by controller design, internal pull-up resistors
10	Efficiency (VRM 8.4. section 1.4)	> 80% at 14.5-A output current. > 40% at 0.5-A output current.	83.5% at 15 A after 12 hours of operation (Figure 8)
11	Overcurrent protection, output short circuit current (VRM 8.4. section 1.5)	Withstands a continuous short circuit of the output	Converter shuts down if the load current exceeds 22 A or shorts. Restarts by cycling V_{CC} voltage.
12	Overvoltage protection (VRM 8.4. section 1.5)	Latches output off if V_{out} = 110 to 125% of nominal	Internal overvoltage protection if V_{out} = 112 to 120% of nominal
13	Maximum component temperature	FETs < 90°C at room temperature with natural cooling	FETs = 72°C, capacitors = 52°C, PCB = 47°C at room temperature of 22°C
14	Dimensions	2.5" x 1.5" x 0.8" (target for embedded regulator, not for VRM 8.4)	2.0" x 1.5" x 0.8"

TP1 (for DC and transient measurements) is placed in the area occupied by the processor to model the worst-case conditions.

Transient load

The transient load tester (see the upper left corner of the evaluation module in Figure 2) provides the high slew-rate load-current pulses. It includes an oscillator based on the TLC555D timer, a TPS2812D driver, and a FET switch connected in series with paralleled resistors to produce the required load-current transient amplitude. The slew-rate levels during rise and fall times can be adjusted separately by variable resistors. The wire loop in series with the load resistors for inserting a current probe provides accurate load-current measurements during transients.

Figure 3. Steady-state output voltage with active droop compensation for improved transient response

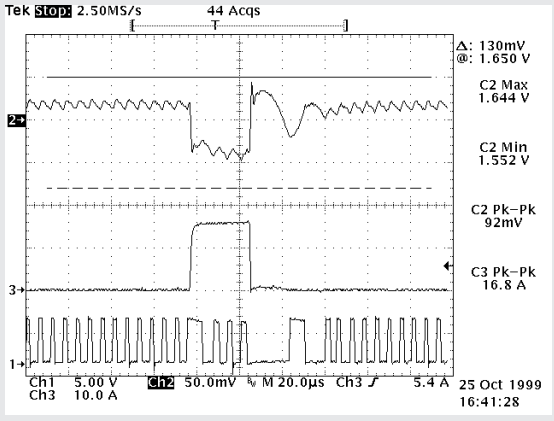


	0	2.5	5	7.5	10	12.5	15	17.5	20
Vin = 4.5 V	1.6237	1.6143	1.6042	1.5937	1.5828	1.5713	1.5596	1.5536	1.542
Vin = 5 V	1.6236	1.6143	1.6042	1.5935	1.5827	1.571	1.5594	1.5519	1.5402
Vin = 5.5 V	1.6236	1.614	1.6037	1.593	1.5818	1.5707	1.5598	1.5515	1.5418

Test results comparison with Intel requirements for VRM 8.4

The design of the SLVP147 EVM is based on the electrical specifications of the Intel document "VRM 8.4 DC-DC Converter Design Guidelines" for >733-MHz clock and 133-MHz bus-frequency Celeron processors. The simplified block diagram of the test setup and the EVM itself are shown in Figure 2.

Figure 4. The output-voltage transient response waveforms measured at test point TP1



The cursors show the limits for this test: 1.52 V minimum and 1.65 V maximum. Ch2 shows output voltage (50 mV/div.), Ch3 shows load current (10 A/div.), and Ch1 shows drain-source voltage (5 V/div.).

All measurements were made at room temperature. During transient tests with 16.8-A load-current steps, the electronic load has been set at 0.8 A to preload the power supply in accordance with VRM 8.4 specification. The VRM 8.4 requirements and test data are shown in Table 1.

Detailed test results and main waveforms

Steady-state output voltage

The steady-state output voltage, measured at test point TP1 at 0- to 20-A load current and 4.5- to 5.5-V input-voltage range, is shown in Figure 3. (The peak load current for this application is 18.4 A.) The line regulation is less than 0.1% (1.6-mV tolerance over the entire input-voltage range). The output voltage depends on the load current because active droop compensation has been used to improve the output-voltage transient tolerance and reduce the number of bulk capacitors. The total voltage droop is 83.5 mV for a current range from 0 to 20 A. Resistor divider R13, R14 sets the 75-mV active droop at a load current of 20 A. The remaining portion of droop (83.5 – 75 = 8.5 mV) relates to the load regulation and droop through supply trace resistance. To compensate the droop, the output voltage had been increased 24 mV above the nominal 1.6 V. It is obvious from Figure 3 that the output voltage is well inside the VRM8.4 specification for a static condition, which is 1.52 V minimum and 1.64 V maximum measured through the microprocessor pins.

Load-current transient response

The output-voltage waveform during the load-current step-up and step-down 16.8-A transition is shown in Figure 4. In accordance with VRM8.4 requirements, the power supply is preloaded by a 0.8-A DC current, which is not included in the load-current transient waveform. The

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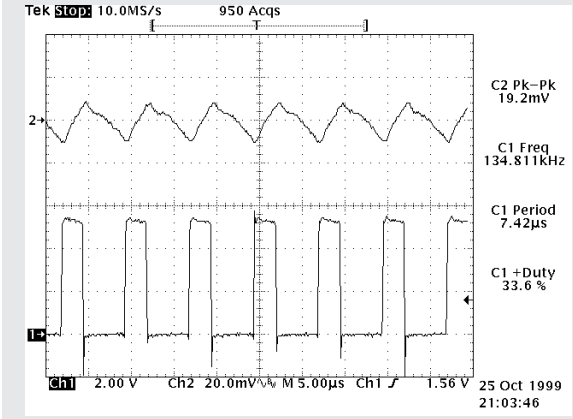
load-current slew rate is 40 A/µs during step-down and 20 A/µs during step-up. The maximum slew rate during load-current step-up is restricted by the stray inductance of the transient tester paths. The peak-to-peak output-voltage amplitude is 92 mV using four 4SP560M OS-CON capacitors. The output-voltage transient lasts only 7 µs for step-up and 34 µs for step-down, which is much less than the 100-µs recovery time from VRM 8.4 requirements.

Special attention has been paid to study the delays between the output-voltage transient and the turn-on of the corresponding FET to see the fast transient response of the hysteretic controller. This delay is 340 ns during the load-current step-down (Figure 5a) and 500 ns during step-up (Figure 5b). Theoretically a voltage mode or current mode controller starts reacting to transients only at the next switching period. To get the same reaction time, these controllers have to run at a switching frequency of over 2 MHz. One can see that the hysteretic controller changes duty cycle in the same switching period when the load-current transient occurs.

Output-voltage ripple and switching frequency range

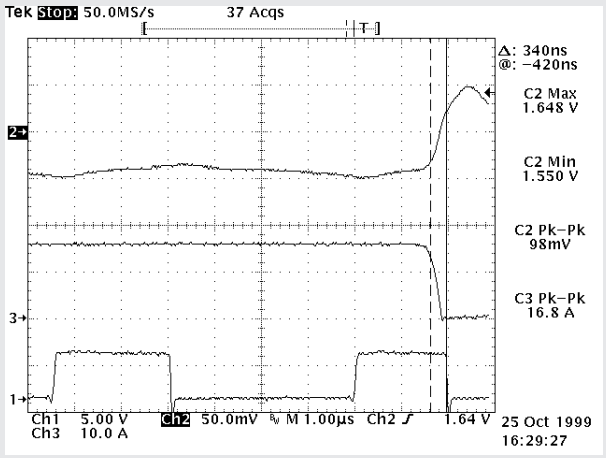
The output-voltage ripple and low-side FET drain-source voltage waveforms are shown in Figure 6. The maximum peak-to-peak ripple does not exceed 20 mV.

Figure 6. Output-voltage ripple and low-side FET drain-source voltage at V_{in} = 5 V, I_{out} = 18 A

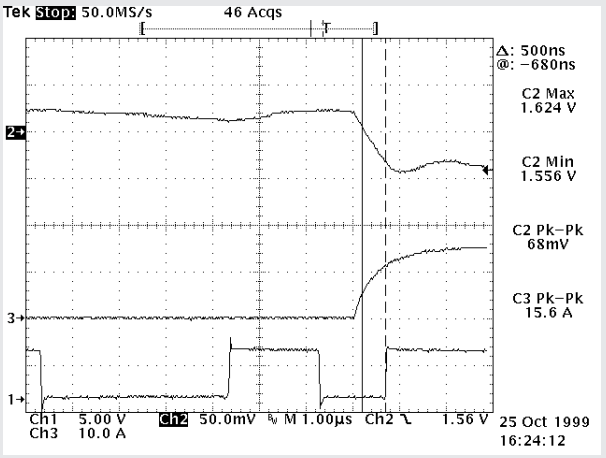


Ch2 shows output-voltage ripple (20 mV/div.), and Ch1 shows drain-source voltage (2 V/div.).

Figure 5. Expanded waveforms during the load-current step-down (a) and step-up (b)



(a)



(b)

The cursors show the 340-ns (a) and 500-ns (b) delays to turn the corresponding FET on after the transient occurs. Ch2 shows output voltage (50 mV/div.), Ch3 shows load current (10 A/div.), and Ch1 shows drain-source voltage (5 V/div.).

The frequency variation is within 135 to 175 kHz over the entire input-voltage and output-current range (see Figure 7). The switching frequency for hysteretic controllers depends on input and output voltage and output filter characteristics. The precise equation for the switching frequency, confirmed by experiments, is represented in TI's application report, "Designing Fast Response Synchronous Buck Converters Using the TPS5210," literature number SLVA044.

Efficiency, power losses, and temperature of components

Efficiency and power losses over the entire input-voltage and output-current range are shown in Figures 8a and 8b. These measurements were made after 12 hours of operation when the temperature of the PCB and components had stabilized. An additional power loss of 0.24 W from the 12-V input is also counted. Efficiency at 15-A load current is 82.8% and, at 0.5 A, is 60.5%. This exceeds specification requirements of 80% and 40%, respectively. The maximum power losses at 15-A load current do not exceed 4.85 W.

The temperature measurements of the main components are shown in Table 2. The measurements were made at a room temperature of 22°C with 5-V input voltage and 14.5-A load current. The cooling conditions were natural without airflow in accordance with the specification. The maximum temperature rise is 50°C on the high-side FET, while the temperature rise of the PCB itself is 25.8°C. These are reasonable values; nevertheless, it is very possible that because the real motherboard has a much larger cooling area, the components will have a lower temperature in the system.

One can see that there is no big difference in temperature of the parallel capacitors, meaning that there is almost equal current sharing between them. The temperature of most components is very close to the PCB temperature.

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Table 2. Temperature measurement results

COMPONENT	PCB	Q1, HIGH-SIDE FET	Q2, LOW-SIDE FET	L1, INPUT IND.	L2, OUTPUT IND.	U1, CONTROLLER	INPUT CAPACITORS			OUTPUT CAPACITORS			
							C1	C2	C3	C5	C6	C7	C8
Temp. (°C)	47.8	72	70	45	50.5	47.5	51.2	48.3	48.3	44.7	45.5	41.3	41
Temp. Rise (°C)	25.8	50	48	23	28.5	25.5	29.2	26.3	26.3	22.7	23.5	19.3	19

Figure 7. Switching frequency variation over the entire input-voltage and output-current range

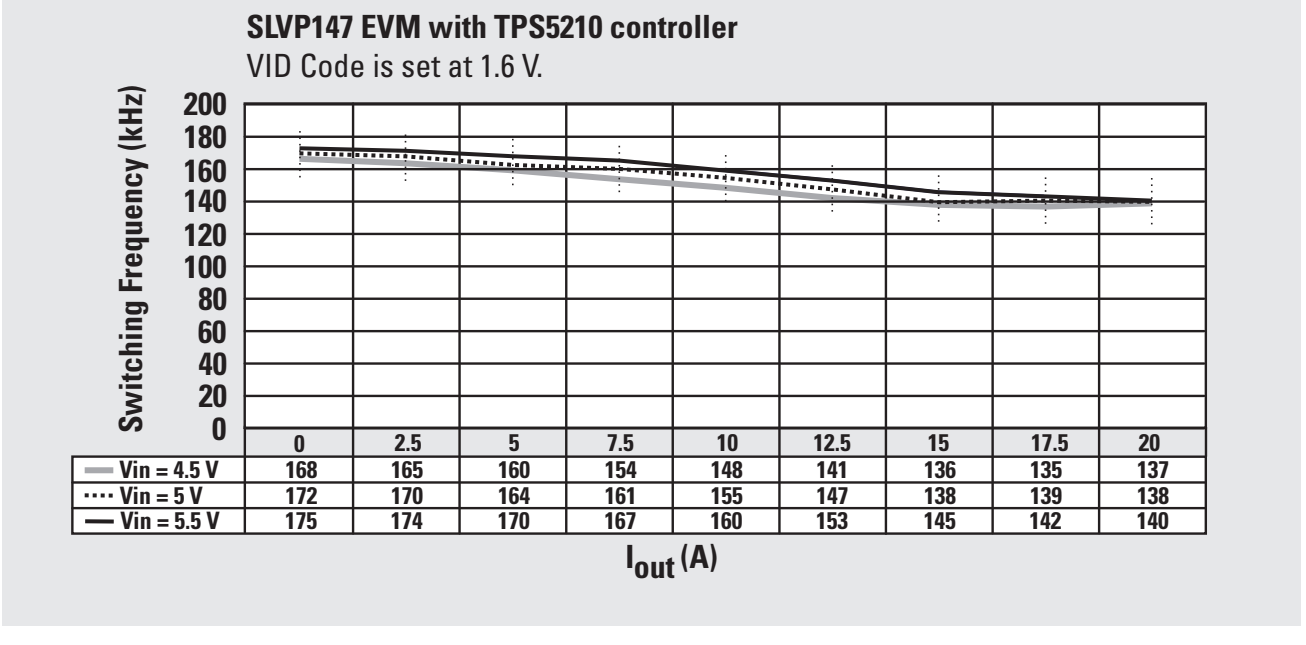

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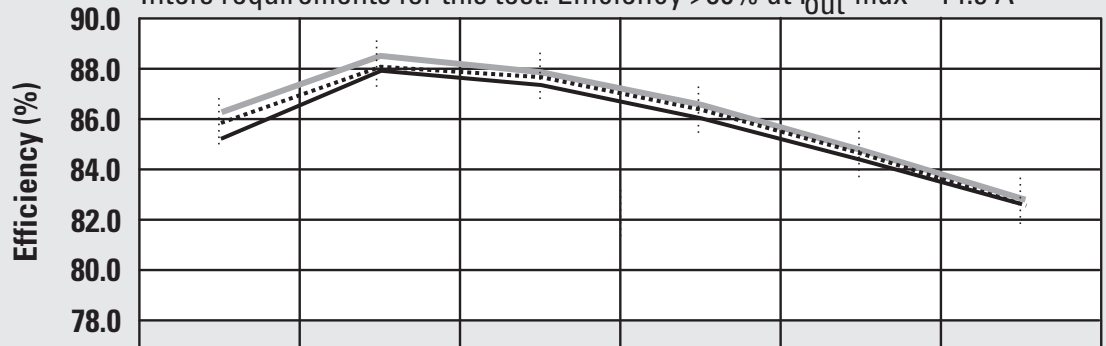
Figure 8. Efficiency (a) and power losses (b) over the entire input-voltage and output-current range after 12 hours of operation

SLVP147 EVM with TPS5210 controller

VID Code is set at 1.6 V Power losses 0.24 W from V_{cc} = 12 V are added.

Intel's requirements for this test: Efficiency >80% at I_{out} max = 14.5 A



	2.5	5	7.5	10	12.5	15
Vin = 4.5 V	86.5	88.8	88.1	86.8	85.0	83.0
Vin = 5 V	86.1	88.3	87.9	86.6	84.8	82.8
Vin = 5.5 V	85.4	88.1	87.6	86.2	84.6	82.8

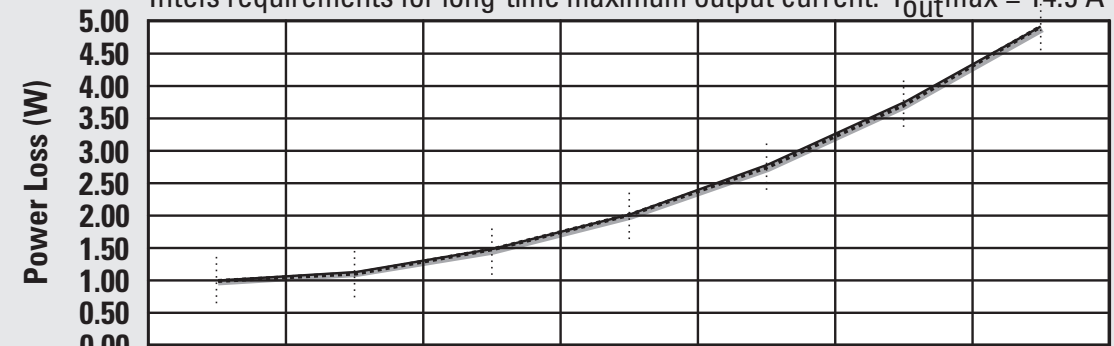
I_{out} (A)

(a)

SLVP147 EVM with TPS5210 controller

VID Code is set at 1.6 V Power losses 0.24 W from V_{cc} = 12 V are added.

Intel's requirements for long-time maximum output current: I_{out} max = 14.5 A



	0	2.5	5	7.5	10	12.5	15
Vin = 4.5 V	0.50	0.63	1.02	1.62	2.41	3.48	4.78
Vin = 5 V	0.53	0.65	1.06	1.65	2.45	3.51	4.85
Vin = 5.5 V	0.55	0.69	1.08	1.70	2.52	3.58	4.85

I_{out} (A)

(b)

The TPS5210 controller has an internal drive-voltage regulator with an 8-V output to decrease power losses in the drive circuitry. These power losses are only 0.24 W in this application. The drain-source voltage of the low-side FET and gate voltages of both FETs are shown in Figure 9.

It is very important to avoid shoot-through current through the power FETs in a synchronous buck converter. The shoot-through current significantly increases power losses and drops reliability. The TPS5210 has active dead-time control to avoid this problem. The waveforms in Figure 10 illustrate that there are optimum delays between turning off the FET and turning on the synchronous FET at all load-current conditions.

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Figure 9. The drain-source voltage of low-side FET and gate voltages of both FETs at V_{in} = 5 V, I_{out} = 18 A

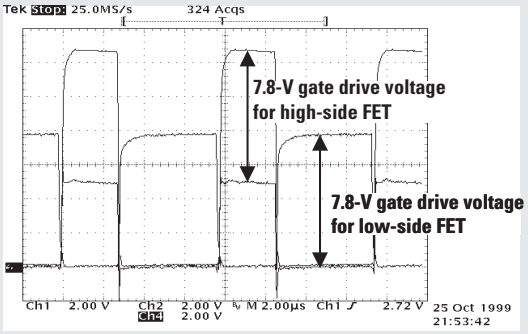
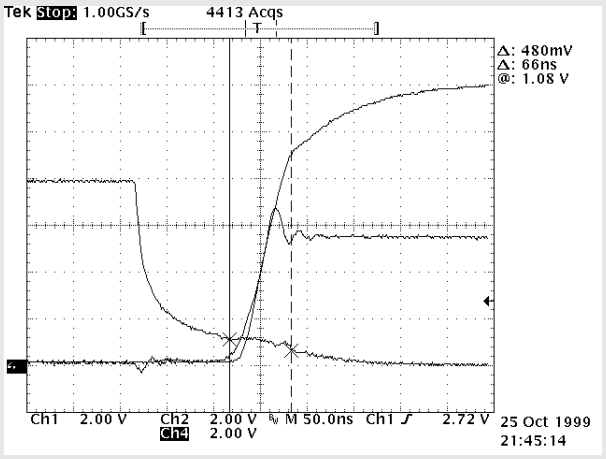
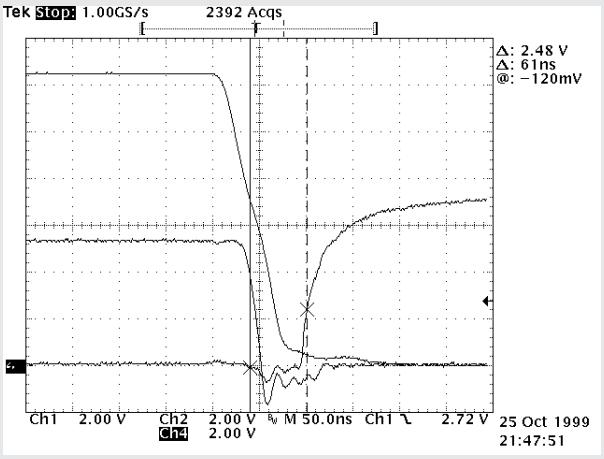


Figure 10. Switching waveforms at I_o = 0 A (a) and (b) and I_o = 18 A (c) and (d)



(a)



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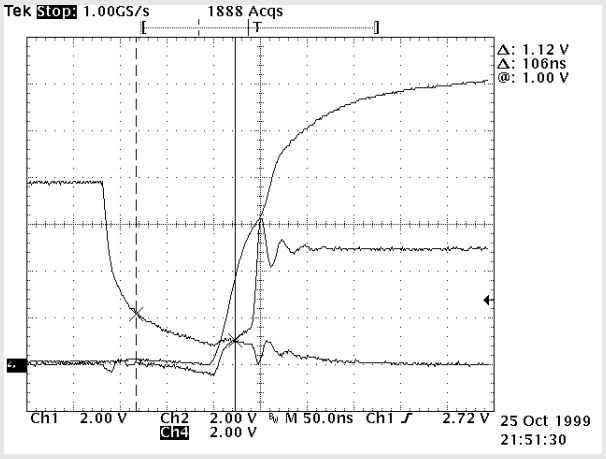
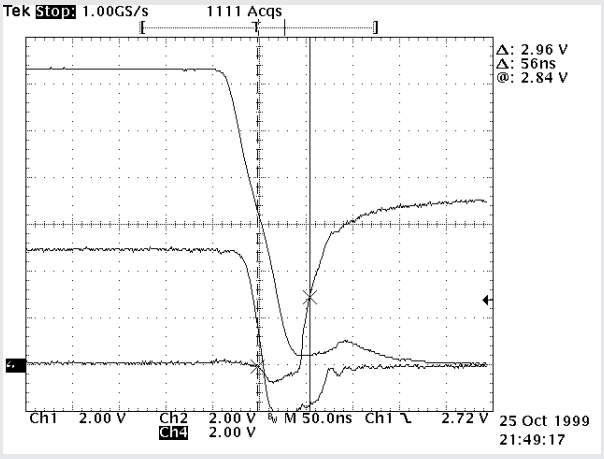


(c)



(d)

The cursors show the delay times.
(a) and (c): Low-side FET turns off, high-side FET turns on. (b) and (d): High-side FET turns off, low-side FET turns on.

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Start-up and relative overshoot

Start-up by applying 12-V V_{CC}, while the enable signal and 5-V input voltage are available, is shown in Figure 11a. Start-up by applying the enable signal, while the 5-V input voltage and 12-V V_{CC} are available, is represented in Figure 11b. The overshoot during start-up does not exceed 1.3%, which is well below the required 10%. The output-voltage rise time does not depend on the load current and has a linear ramp form. In this application, rise time was set at about 9 ms by the external capacitor.

Conclusions

- The SLVP147 evaluation module with the TPS5210 hysteretic controller meets the electrical specification of the Intel document "VRM 8.4 DC-DC Converter Design Guidelines."
- The hysteresis window, active droop, and output-voltage set point have been optimized for applications with over 733-MHz clock and 133-MHz bus-frequency Celeron-type processors.
- The load-current transient tests implemented in the EVM transient tester have shown excellent dynamic characteristics of the TPS5210 hysteretic controller for desktop applications using the minimum number of bulk OS-CON capacitors.
- The component temperature measurements in worst-case cooling conditions have given reasonable results.

References

For more information related to this article, visit the TI Web site at www.ti.com/ and look for the following materials by entering the TI literature number into the quick-search box. References without a TI literature number should be available through traditional publishing outlets.

Document Title	TI Lit. #
1. "TPS5210 Programmable Synchronous-Buck Regulator Controller," September 1998 revised May 1999	SLVS171A
2. "TPS5211 High Frequency Programmable Synchronous-Buck Regulator Controller," September 1999	SLVS243
3. "Designing Fast Response Synchronous Buck Regulator Using the TPS5210," Application Report, March 1999	SLVA044
4. "VRM 8.4 DC-DC Converter Design Guidelines," Intel Corporation, November 1999, order number 245335-001.	—
5. R. Miftakhutdinov, "Analysis of Synchronous Buck Converter with Hysteretic Controller at High Slew-Rate Load Current Transients," *Proc. of High Frequency Power Conversion Conference*, 1999, pp. 55-69.	—

Related Web sites

www.ti.com/sc/docs/products/msp/pwrmgmt/index.htm

www.ti.com/sc/docs/tools/analog/powermanagementdevelopmentboards.html

Get product data sheets at:

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Replace *device* with tlc555, tps2812, tps5210, or tps5211

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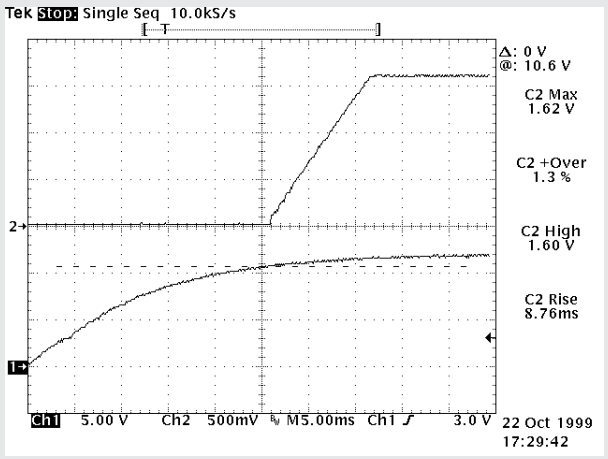
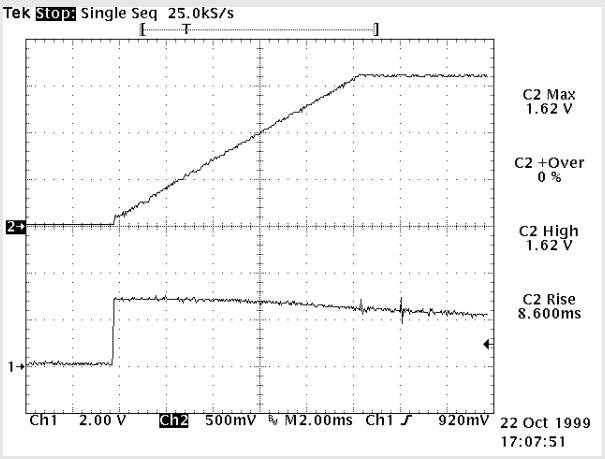
Figure 11. Start-up by applying V_{CC} voltage (a) and the enable signal (b)



(a)



(b)

The cursor shows the undervoltage lockout level.
(a): Ch1 shows V_{CC} voltage (5 V/div.), and Ch2 shows output voltage (0.5 V/div.).
(b): Ch1 shows the enable signal (2 V/div.), and Ch2 shows the output voltage (0.5 V/div.).

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